What is claimed is:

1. ~~An instruction processing device, comprising:~~

a storage circuit storing address mode information of a fetched instruction with an instruction address of the fetched instruction;

a branch instruction control circuit controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the address mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

2. The instruction processing device according to claim 1, wherein said branch instruction control circuit stores address mode information of a branch destination of the branch instruction with an ~~instruction address of the branch destination.~~

3. The instruction processing device according to claim 2, wherein said branch instruction control circuit generates the address mode information of the branch destination based on the address mode

information of the branch instruction.

4. The instruction processing device according to claim 2, wherein said branch instruction control circuit judges whether address mode information and an instruction address of a branch destination predicted by a branch prediction are correct using the address mode information and instruction address of the branch destination.

5. The instruction processing device according to claim 2, wherein said branch instruction control circuit outputs a signal indicating the address mode information and instruction address of the branch destination when issuing a branch destination instruction fetch request.

6. The instruction processing device according to claim 1, wherein said branch instruction control circuit outputs a signal indicating whether the branch instruction is accompanied by an address mode change when control of the branch instruction is terminated.

7. The instruction processing device according to claim 1, further comprising

a branch history circuit relating address mode information and an instruction address of a branch instruction to address mode information and an instruction address of a branch destination, storing related address mode information and instruction addresses of the branch instruction and branch destination, and making a branch prediction for the fetched branch instruction.

8. The instruction processing device according to claim 1, further comprising

a branch destination address generation circuit generating an instruction address of a branch destination of the branch instruction using the address mode information,

wherein said transfer circuit transfers the address mode information stored in the storage circuit to the branch destination address generation circuit when the branch instruction is executed.

9. ~~An instruction processing device, comprising:~~

a storage circuit storing mode information of a fetched instruction with an instruction address of the fetched instruction;

a branch instruction control circuit controlling

a branch instruction using the mode information if the fetched instruction is the branch instruction; and

a transfer circuit transferring the mode information stored in the storage circuit to the branch instruction control circuit when the branch instruction is executed.

10. An instruction processing device, comprising:

a fetch circuit fetching an instruction;

a storage circuit storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction; and

a control circuit controlling an instruction process of each instruction based on the stored mode information.

11. An instruction processing device provided with a plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

a storage circuit storing mode information obtained when an instruction fetch request is issued, with an instruction address for each port; and

a fetch circuit performing an instruction fetch based on mode information corresponding to a port to

~~be used.~~

12. An instruction processing method, comprising:

handling mode information of an information processing apparatus, which is to be determined when fetching each instruction, as a part of an instruction address;

fetching an instruction;

storing mode information of the fetched instruction in each cycle of an instruction process for the fetched instruction; and

controlling the instruction process for the fetched instruction based on the stored mode information.

13. An instruction processing device, comprising:

storage means for storing address mode information of a fetched instruction with an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the address mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the address mode information stored in the storage means to the branch

instruction control means when the branch instruction is executed.

14. An instruction processing device, comprising:

storage means for storing mode information of a fetched instruction with an instruction address of the fetched instruction;

branch instruction control means for controlling a branch instruction using the mode information if the fetched instruction is the branch instruction; and

transfer means for transferring the mode information stored in the storage means to the branch instruction control means when the branch instruction ~~is executed.~~

15. An instruction processing device, comprising:

fetch means for fetching an instruction;

storage means for storing mode information of each fetched instruction as a part of an instruction address of the fetched instruction; and

control means for controlling an instruction process of each instruction based on the stored mode information.

16. ~~An instruction processing device provided with a~~

plurality of instruction fetch ports and performing an instruction fetch by way of an out-of-order system, comprising:

storage means for storing mode information obtained when an instruction fetch request is issued, with an instruction address for each port; and

fetch means for performing an instruction fetch based on mode information corresponding to a port to be used.

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